



SSC8415GS6

P-Channel Enhancement Mode MOSFET

➤ Features

V _{DS}	V _{GS}	R _{DS(ON)} Typ.	I _D
-20V	±12V	35mΩ @-4V5	-4A
		44mΩ @-2V5	

➤ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

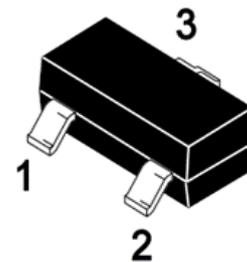
➤ Applications

- Load Switch
- Portable Devices
- DCDC Conversion

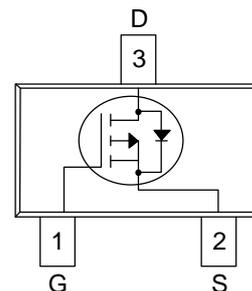
➤ Ordering Information

Device	Package	Shipping
SSC8415GS6	SOT-23	3000/Reel

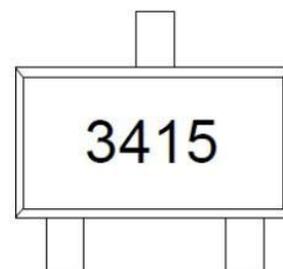
➤ Pin configuration



SOT-23



Pin Configuration (Top View)



Marking



➤ **Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-20	V
V_{GSS}	Gate-to-Source Voltage	± 12	V
I_D	Continuous Drain Current ^a	-4	A
I_{DM}	Pulsed Drain Current ^b	-22	A
P_D	Power Dissipation ^c	0.9	W
P_{DSM}	Power Dissipation ^a	0.55	W
T_J	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a	140	$^{\circ}\text{C}/\text{W}$

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user is specific board design. The power dissipation is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

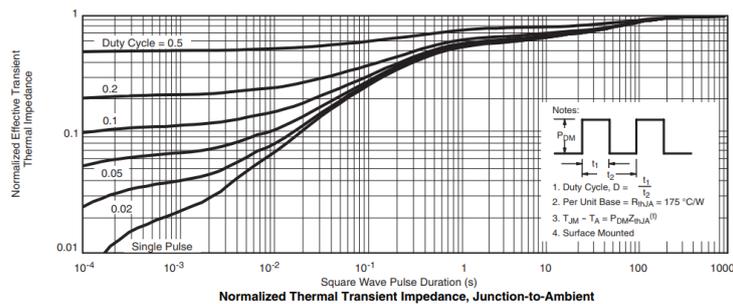
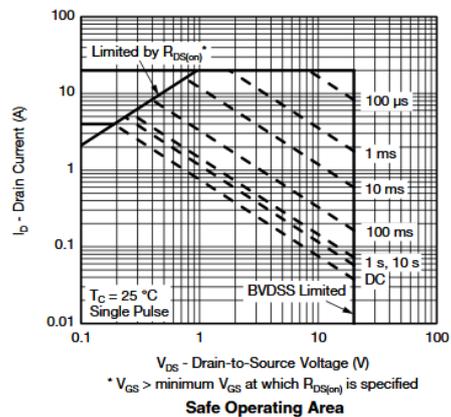
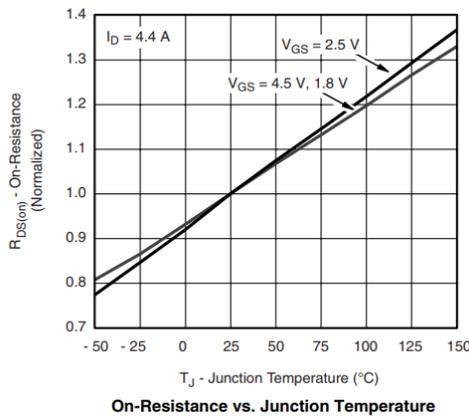
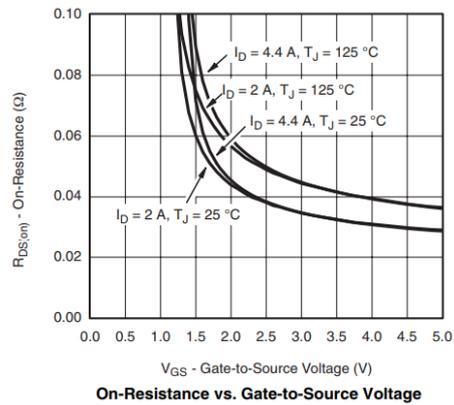
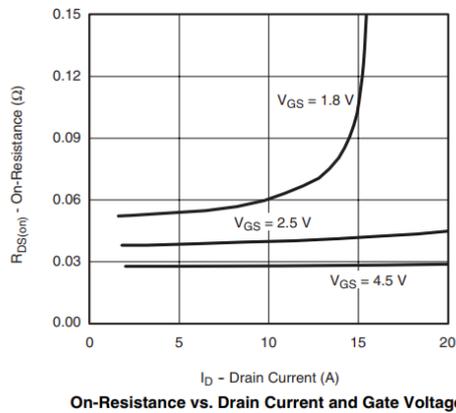
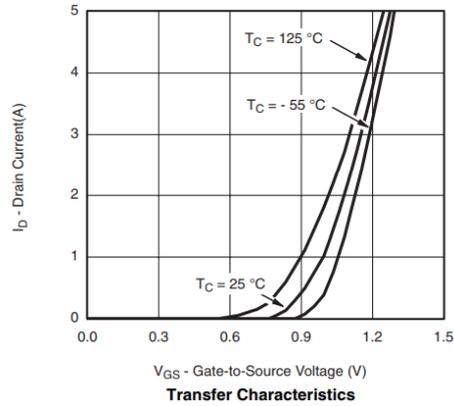
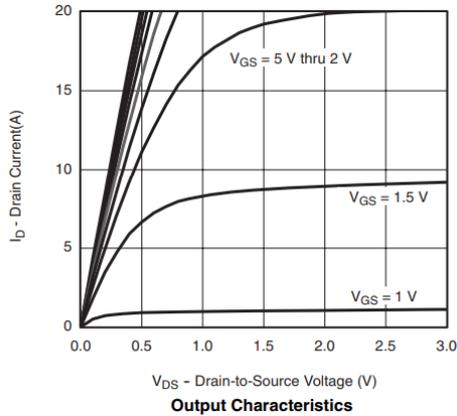


➤ **Electrical Characteristics (T_A=25°C unless otherwise noted)**

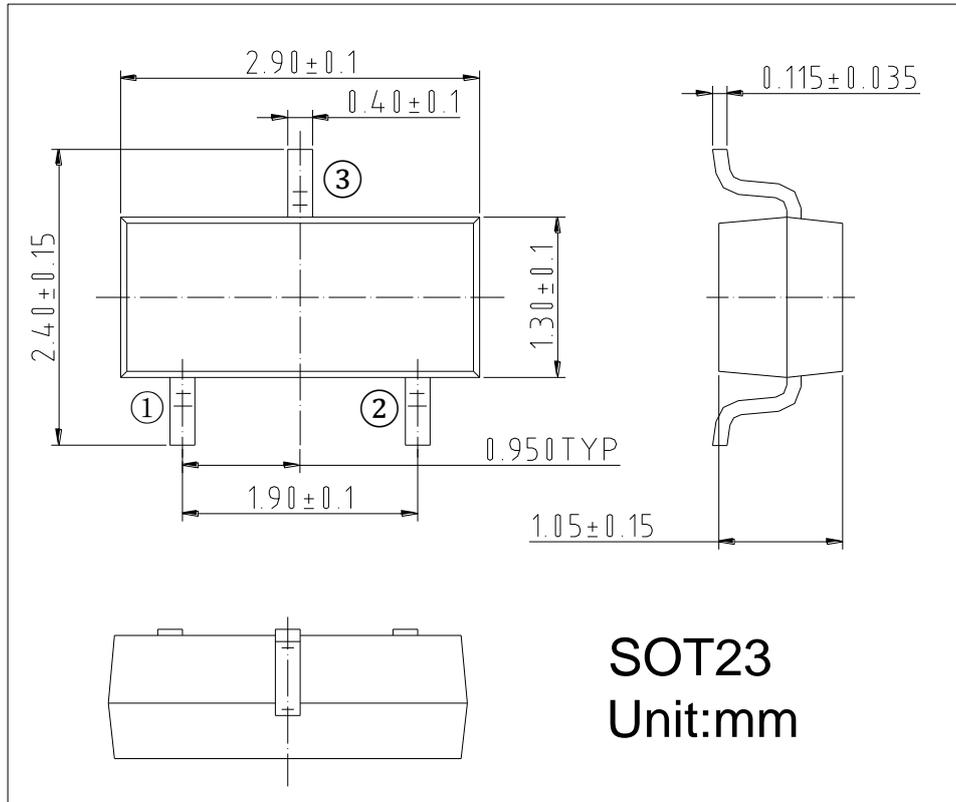
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-10uA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.4	-0.6	-0.9	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-3.5A		35	40	mΩ
		V _{GS} =-2.5V, I _D =-3A		44	65	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			-1	μA
Gate-Source Leak Current	I _{GSS}	V _{GS} =±12V, V _{DS} =0V			±100	nA
Forward Voltage	V _{SD}	V _{GS} =0V, I _S =-1.6A	-0.5	-0.75	-1.2	V
Input Capacitance	C _{ISS}	V _{DS} = -10V, V _{GS} = 0V, f = 1MHz		869		pF
Output Capacitance	C _{OSS}			265		
Reverse Transfer Capacitance	C _{RSS}			258		
Turn-on Delay Time	T _{D(ON)}	V _{DS} =-10V, I _D =-1.0A, R _L =6Ω, V _{GS} =-4.5V, R _G =6Ω,		12		ns
Rise Time	T _r			8.9		
Turn-off Delay Time	T _{D(OFF)}			45		
Fall Time	T _f			15		
Total Gate Charge	Q _G	V _{DS} =-10V, V _{GS} =-4.5V, I _D =-5A		12		nC
Gate to Source Charge	Q _{GS}			2.1		
Gate to Drain Charge	Q _{GD}			2.4		



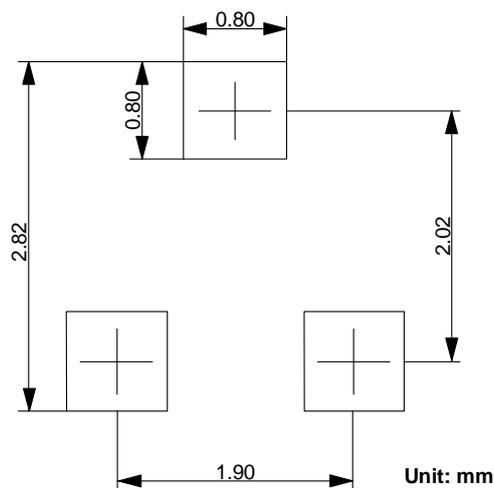
➤ Typical Performance Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)



➤ Package Information



➤ Recommended Pad outline





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